Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims of the application:

Listing of claims:

1. (Currently amended) A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer such that none of said horizontal trenches completely intersects any of said vertical trenches and separating said dielectric layer into cells, whose dimensions are small compared to dimensions of a bonding pad, such that cracks will not propagate in any direction much beyond a cell before being stopped by a trench in order to limit the propagation of any cracks that may form;

filling said trenches with a conducting material and performing CMP over said dielectric layer and said filled trenches to obtain a top surface;

depositing bonding metal patterns over said top surface;

bonding wires onto said bonding metal patterns;

forming a passivation layer over said top surface and said bonding layer patterns.

2. (Original) The method of Claim 1 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.
3. (Original)The method of Claim 1 wherein said dielectric layer is a composite of dielectric layers.
4. (Canceled)
5. (Original)The method of Claim 1 wherein said dielectric layer is a composed of two layers, an oxide layer formed using SACVD and an oxide layer formed using HSTEOS.
6. (Original) The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a plug process.
7. (Original) The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.
8. (Previously presented) The method of Claim 1 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: Al plug, Cu plug, silicide plug.
9. (Original)The method of claim 1 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

10. (Original)The method of claim 1 wherein the separation between neighboring horizontal trenches and neighboring vertical trenches is between 0.2 and 20 micrometers.

11. (Currently amended) A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer according to the nonintersecting layout, with separations between said vertical trenches and separations between said horizontal trenches being small compared to dimensions of a bonding pad, such that cracks will not propagate in any direction much beyond the length of said separations before being stopped by a trench, thus limiting the propagation of any cracks that may form;

filling said trenches with a conducting material and performing CMP over said dielectric layer and said filled trenches to obtain a top surface;

depositing bonding metal patterns over said top surface;

bonding wires onto said bonding metal patterns;

forming a passivation layer over said top surface and said bonding layer patterns.

12. (Original)The method of Claim 11 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.

13. (Original)The method of Claim 11 wherein said dielectric layer is a composite of dielectric layers.

14. (Canceled).

15. (Canceled)

16. (Original)The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a plug process.

17. (Original) The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.

18. (Previously presented) The method of Claim 11 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: Al plug, Cu plug, silicide plug.

19. (Original)The method of claim 11 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

20. (Previously presented) The method of claim 11 wherein the separation between neighboring horizontal trenches and neighboring vertical trenches is between 0.1 and 10 micrometers, and the ratio between the spacing of perpendicular trenches to the spacing of parallel trenches is less than about 1/5, and the spacing of perpendicular trenches is greater than about 0.1 micrometers

21. (Currently amended) A method of forming a bonding pad that is immune to IMD cracking, comprising:

providing a partially processed semiconductor wafer having all metal levels completed;

forming a blanket dielectric layer over the uppermost metal level;

patterning and etching said dielectric layer to form horizontal and vertical arrays of trenches passing through said dielectric layer according to the brick laying layout or the modified brick laying layout, with separations between said vertical trenches and separations between said horizontal trenches being small compared to dimensions of a bonding pad, such that cracks will not propagate in any direction much beyond the length of said separations before being stopped by a trench, thus limiting the propagation of any cracks that may form;

filling said trenches with a conducting material and performing CMP over said dielectric layer and said filled trenches to obtain a top surface;

depositing bonding metal patterns over said top surface;

bonding wires onto said bonding metal patterns;

forming a passivation layer over said top surface and said bonding layer patterns.

22. (Original)The method of Claim 21 wherein said dielectric layer is composed of materials from the set: silicon oxide, silicon nitride, silicon oxynitride.

23. (Original)The method of Claim 21 wherein said dielectric layer is a composite of dielectric layers.

24. (Canceled).

25. (Canceled)

26. (Original)The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a plug process.

27. (Original)The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a W plug process.

28. (Previously presented) The method of Claim 21 wherein the filling of said trenches with a conducting material is accomplished using a plug process from the set: Al plug, Cu plug, silicide plug.

29. (Original) The method of claim 21 wherein the width of said trenches is between 0.1 and 0.5 micrometers.

30. (Original) The method of claim 21 wherein the separation between neighboring horizontal trenches is between 0.1 and 10 micrometers and neighboring vertical trenches is between 0.1 and 10 micrometers.

31. (Original) The method of Claim 21 wherein the overlap area in said modified bricklaying layout is between 0.1 and 1 of the overlap area of said bricklaying layout.